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EXAMINER	
SPITTLE, MATTHEW D	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

5

Office Action Summary	Application No.	Applicant(s)
	10/662,034	MANTEY ET AL.
	Examiner	**Art Unit**
	Matthew D. Spittle	2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 42-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 42-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 13, and 42 – 44 have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 12 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 12 recites, "...a send machine coupled between a host processor and the bus controller over the second internal bus..." and "...the second FIFO further coupled between the host processor and the bus controller over the second internal bus..." Reviewing Applicant's Figure 2A as well as the arguments on page 20, lines 8 – 10 reveal that the internal bus (such as items 254, 256, 212) that connects the send machine between the bus controller and the host processor, and the internal bus (assuming it to be 242, 246 and 224) are ***not*** the same buses, and thus, the claim recites a structure which is not enabled by the disclosure. For purposes of examination, Examiner will assume Applicant has meant to claim a **third internal bus** (242, 246, 224 as an example) that connects the second FIFO between the host processor and the bus controller.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (U.S. 6,122,758) in view of Elliot (U.S. Pub. 2005/0055489).

Regarding claim 1, Johnson et al. describe a computer system comprising:

A system bus implemented in accordance with an Inter-IC bus specification (Figure 4, 7, item 310; column 7, lines 10 – 12);

A bus controller coupled to the system bus (where a bus controller may be interpreted as a system interface processor; column 11, lines 31 – 36, 61 - 65) and to an internal bus (Fig. 4, 7, item 226);

A send machine (Fig. 7, item 707) and a FIFO buffer coupled to the send machine (Fig. 7, 516), however Johnson et al. fails to teach the send machine and FIFO buffer connected as recited in the claim.

Elliot teaches a bridge circuit which could be implemented in a system such as that of Johnson et al. for the purpose of allowing components to operate at different clock rates (par. 4). This circuit could be implemented in Johnson et al., for example, in the location of items 514 and 516 in Figure 7 to allow the system interface processor (312) and host processor (200) to operate at different clock rates. Thus, the combination of Johnson et al. and Elliot teaches a send machine (Elliot: 68) coupled between a host processor (Johnson: 200) and the bus controller (Johnson: 312) over a second internal bus (Elliot: I-data, t-data, I-add, t-add); and a first first-in first-out (FIFO) buffer (Elliot: 60) coupled to the send machine (Elliot: 68), the first FIFO further coupled in parallel with the send machine (as shown in Elliot, Fig. 2) between the host processor (Johnson: 200) and the bus controller (Johnson: 312) over the first internal bus (Johnson: 226) but not over the system bus (Johnson: 310).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the bridge circuit as taught by Elliot into the system of Johnson et al. for the purpose of allowing different components on the bus to correctly operate at different clock rates (par. 4). This would have been obvious since Elliot teaches that it is advantageous to operate components at different clock rates in an integrated circuit (par. 4).

Regarding claim 2, Elliot teaches the additional limitation wherein the first FIFO buffer comprises means for receiving a plurality of bytes from the host processor without interrupting the host processor (par. 6, par. 34).

Regarding claim 3, Elliot teaches the additional limitation wherein:

The first FIFO buffer comprises means for receiving a plurality of bytes from the host processor (par. 6, par. 34);

The send machine comprises means for transmitting the plurality of bytes over the system bus without interrupting the host processor (par. 30).

Regarding claim 4, Elliot teaches the additional limitation comprising:

A receive machine (70)) coupled between the host processor and the bus controller;

A second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller (62).

Regarding claim 12, Johnson et al. describe a computer system comprising:

A system bus implemented in accordance with an Inter-IC bus specification (Figure 4, 7, item 310; column 7, lines 10 – 12);

A bus controller coupled to the system bus (where a bus controller may be interpreted as a system interface processor; column 11, lines 31 – 36, 61 - 65) and to an internal bus (Fig. 4, 7, item 226);

A send machine (Fig. 7, item 707) and a FIFO buffer coupled to the send machine (Fig. 7, 516), however Johnson et al. fails to teach the send machine and FIFO buffer connected as recited in the claim.

Elliot teaches a bridge circuit which could be implemented in a system such as that of Johnson et al. for the purpose of allowing components to operate at different clock rates (par. 4). This circuit could be implemented in Johnson et al., for example, in the location of items 514 and 516 in Figure 7 to allow the system interface processor (312) and host processor (200) to operate at different clock rates. Thus, the combination of Johnson et al. and Elliot teaches a send machine (Elliot: 68) coupled between a host processor (Johnson: 200) and the bus controller (Johnson: 312) over a second internal bus (Elliot: I-data, t-data, I-add, t-add); and a first first-in first-out (FIFO) buffer (Elliot: 60) coupled to the send machine (Elliot: 68), the first FIFO further coupled in parallel with the send machine (as shown in Elliot, Fig. 2) between the host processor (Johnson: 200) and the bus controller (Johnson: 312) over the first internal bus (Johnson: 226) but not over the system bus (Johnson: 310).

Additionally, Elliot teaches A receive machine (70)) coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor (par. 6, par. 34); and a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller (62) over the **third** internal bus (I-r-data, t-r-data), the second FIFO not being coupled to the receive machine over the second internal bus (as shown in Fig. 2) but not over the system bus (as shown in Fig.

2), the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor (par. 44).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the bridge circuit as taught by Elliot into the system of Johnson et al. for the purpose of allowing different components on the bus to correctly operate at different clock rates (par. 4). This would have been obvious since Elliot teaches that it is advantageous to operate components at different clock rates in an integrated circuit (par. 4).

* * *

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (U.S. 6,122,758) in view of Elliot (U.S. Pub. 2005/0055489). and Yoshida (U.S. 5,928,372).

Johnson et al. fail to teach wherein the receive machine comprises checksum generation means for generating a message checksum for a message while the message is being received by the bus controller over the system bus.

Yoshida teaches a checksum generation means for generating a message checksum for a message while the message is being received by the bus controller over the system bus (where checksum generation means may be interpreted as data check code generation circuits; column 11, lines 14 – 24).

It would have been obvious to one or ordinary skill in this art at the time of invention by applicant to combine the checksum generation means of Yoshida with the system of Johnson et al. and Elliot in order to provide for a means of verifying the data transmitted across the system bus. This would have been obvious since error-free data is critical to the correct operation of a digital system.

* * *

Claims 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (U.S. 6,122,758) in view of Elliot (U.S. Pub. 2005/0055489).and Feeney et al. (U.S. 6,072,781).

With regard to claim 6, Johnson et al. describe the computer system of claim 1, further comprising:

Means for receiving a message from the host processor (Figure 7, items 516, 707; column 12, lines 26 – 32);

Means for attempting to send the message over the system bus to a target device (column 15, lines 15 – 36 give an example of how a message is sent over the system bus to a target device (microcontroller)).

Means for determining whether the message was received without errors by the target device (column 15, lines 62 – 64).

Johnson et al. and Elliot fail to describe retry means for attempting again to send the message over the communication bus to the target device if it is determined that the message was not received without errors by the target.

Feeney et al. teach retry means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device (column 16, lines 36 – 49 describe retrying messages that failed to send; column 16, lines 36 – 49 describe retrying a message without involving the processor).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the means of retrying failed messages as taught by Feeney et al. into the computer system of Johnson et al. and Elliot for the purpose of ensuring the delivery of messages on the communication bus.

With regard to claim 7, Feeney et al. teach the additional limitation wherein the retry means comprises means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device (column 16, lines 36 – 49 describe retrying a message without involving the processor).

With regard to claim 8, Feeney et al. teach the additional limitation wherein the retry means comprises means for attempting again to send the message over the system bus to the target device without obtaining the message again from the host

processor if it is determined that the message was not received without errors by the target device (column 16, lines 36 – 49 describe storing the message in a FIFO in order to allow the processor to move onto other tasks).

* * *

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (U.S. 6,122,758) in view of Elliot (U.S. Pub. 2005/0055489) and Cao et al. (U.S. 5,230,044).

Johnson et al. and Elliot fail to teach a busfree count means for storing a busfree count associated with the computer system, a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use, and a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.

Cao et al. teach:

A busfree count means for storing a busfree count (where a busfree count may be interpreted as an arbitration count number; column 4, lines 42 – 50);

A busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the

system bus becomes available for use (where a busfree timer may be interpreted as a "quiet slot" counter; column 4, lines 51 – 60);

A fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal (where a busfree count may be interpreted as an arbitration count number; column 5, lines 59 – 64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the busfree count and busfree timer as taught by Cao et al. into the system of Johnson et al. and Elliot for the purpose of providing arbitration amongst devices on the system bus. This would have been obvious since Cao et al. teach that their invention provides for more efficient use of bus bandwidth (column 10, lines 25 – 59), along with permitting data communication with a very small probability of data collisions (column 4, lines 32 – 34).

* * *

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (U.S. 6,122,758) in view of Elliot (U.S. Pub. 2005/0055489).and Webb et al. (U.S.4,577,060).

With regard to claim 10, Johnson et al. and Elliot fail to teach a byte timer coupled between the bus controller and the host processor.

Webb et al. teach a byte timer (where a byte timer may be interpreted as a no-response timer; column 13, lines 49 - 60).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the byte timer as taught by Webb et al. into the system of Johnson et al. and Elliot. This would have been obvious in order to provide a method of ensuring that a communication link (or bus) is operating properly, and prevent the system from wasting time sending messages to processors/terminals that are not responsive (column 14, lines 11 – 19).

With regard to claim 11, Webb et al. teach the additional limitation wherein the byte timer (interpreted as a no-response timer) comprises means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed (where a host processor may be interpreted as a terminal; where generating a signal indicating the processor has failed may be interpreted as marking a terminal as being “offline” or “down”; column 13, line 49 – column 14, line 30).

* * *

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Elliot, Feeney et al., Cao et al., and further in view of Webb et al.

Johnson et al. teach a computer system of claim 12 further comprising:

Means for receiving a message from the host processor (Figure 7, items 516, 707; column 12, lines 26 – 32);

Means for attempting to send the message over the system bus to a target device (column 15, lines 15 – 36 give an example of how a message is sent over the system bus to a target device (microcontroller)).

Means for determining whether the message was received without errors by the target device (column 15, lines 62 – 64).

Johnson et al. and Elliot fail to describe a retry means, a busfree count means, a busfree count timer, a fair arbitration block, and a byte timer.

Feeney et al. teach retry means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device (column 16, lines 36 – 49 describe retrying messages that failed to send; column 16, lines 36 – 49 describe retrying a message without involving the processor).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the means of retrying failed messages as taught by Feeney et al. into the computer system of Liu et al for the purpose of ensuring the delivery of messages on the communication bus.

Cao et al. teach:

A busfree count means for storing a busfree count (where a busfree count may be interpreted as an arbitration count number; column 4, lines 42 – 50);

A busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use (where a busfree timer may be interpreted as a "quiet slot" counter; column 4, lines 51 – 60);

A fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal (where a busfree count may be interpreted as an arbitration count number; column 5, lines 59 – 64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the busfree count and busfree timer as taught by Cao et al. into the system of Johnson et al., Elliot, and Feeney et al, for the purpose of providing arbitration amongst devices on the system bus. This would have been obvious since Cao et al. teach that their invention provides for more efficient use of bus bandwidth (column 10, lines 25 – 59), along with permitting data communication with a very small probability of data collisions (column 4, lines 32 – 34).

Webb et al. teach a byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed (where a byte timer may be interpreted as a no-response timer; column 13, lines 49 – 60; where a host processor may be interpreted as a terminal; where generating a signal indicating the processor has failed may be interpreted as marking a terminal as being "offline or "down"; column 13, line 49 – column 14, line 30).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the byte timer as taught by Webb et al. into the system of Johnson et al., Feeney et al., and Cao et al. This would have been obvious in order to provide a method of ensuring that a communication link (or bus) is operating properly, and prevent the system from wasting time sending messages to processors/terminals that are not responsive (column 14, lines 11 – 19).

* * *

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Elliot, Feeney et al., Cao et al., and Webb et al.

Regarding claim 42, Johnson et al. teach a computer system comprising:

A system bus implemented in accordance with an Inter-IC bus specification (Figure 4, 7, item 310; column 7, lines 10 – 12);

A bus controller coupled to the system bus (where a bus controller may be interpreted as a system interface processor; column 11, lines 31 – 36, 61 - 65) and to an internal bus (Fig. 4, 7, item 226);

A send machine (Fig. 7, item 707) and a FIFO buffer coupled to the send machine (Fig. 7, 516), however Johnson et al. fails to teach the send machine and FIFO buffer connected as recited in the claim.

Elliot teaches a bridge circuit which could be implemented in a system such as that of Johnson et al. for the purpose of allowing components to operate at different

clock rates (par. 4). This circuit could be implemented in Johnson et al., for example, in the location of items 514 and 516 in Figure 7 to allow the system interface processor (312) and host processor (200) to operate at different clock rates. Thus, the combination of Johnson et al. and Elliot teaches a send machine (Elliot: 68) coupled between a host processor (Johnson: 200) and the bus controller (Johnson: 312) over a second internal bus (Elliot: l-data, t-data, l-add, t-add); and a first first-in first-out (FIFO) buffer (Elliot: 60) coupled to the send machine (Elliot: 68), the first FIFO further coupled in parallel with the send machine (as shown in Elliot, Fig. 2) between the host processor (Johnson: 200) and the bus controller (Johnson: 312) over the first internal bus (Johnson: 226) but not over the system bus (Johnson: 310).

Additionally, Elliot teaches A receive machine (70)) coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor (par. 6, par. 34); and a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller (62) over the **third** internal bus (l-r-data, t-r-data), the second FIFO not being coupled to the receive machine over the second internal bus (as shown in Fig. 2) but not over the system bus (as shown in Fig. 2), the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor (par. 44).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the bridge circuit as taught by Elliot into the system of Johnson et al. for the purpose of allowing different components on the bus to

correctly operate at different clock rates (par. 4). This would have been obvious since Elliot teaches that it is advantageous to operate components at different clock rates in an integrated circuit (par. 4).

Johnson et al. additionally teaches means for receiving a message from the host processor (Figure 7, items 516, 707; column 12, lines 26 – 32);

Means for attempting to send the message over the system bus to a target device (column 15, lines 15 – 36 give an example of how a message is sent over the system bus to a target device (microcontroller)).

Means for determining whether the message was received without errors by the target device (column 15, lines 62 – 64).

Johnson et al. and Elliot fail to describe a retry means, a busfree count means, a busfree count timer, a fair arbitration block, and a byte timer.

Feeney et al. teach retry means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device (column 16, lines 36 – 49 describe retrying messages that failed to send; column 16, lines 36 – 49 describe retrying a message without involving the processor).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the means of retrying failed messages as taught by Feeney et al. into the computer system of Johnson et al. for the purpose of ensuring the delivery of messages on the communication bus.

Cao et al. teach:

A busfree count means for storing a busfree count (where a busfree count may be interpreted as an arbitration count number; column 4, lines 42 – 50);

A busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use (where a busfree timer may be interpreted as a "quiet slot" counter; column 4, lines 51 – 60);

A fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal (where a busfree count may be interpreted as an arbitration count number; column 5, lines 59 – 64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the busfree count and busfree timer as taught by Cao et al. into the system of Johnson et al. and Elliot for the purpose of providing arbitration amongst devices on the system bus. This would have been obvious since Cao et al. teach that their invention provides for more efficient use of bus bandwidth (column 10, lines 25 – 59), along with permitting data communication with a very small probability of data collisions (column 4, lines 32 – 34).

Webb et al. teach a byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed (where a byte timer may be interpreted as a no-response timer; column 13, lines 49 – 60; where a host processor may be interpreted as a terminal;

where generating a signal indicating the processor has failed may be interpreted as marking a terminal as being “offline or “down”; column 13, line 49 – column 14, line 30).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the byte timer as taught by Webb et al. into the system of Johnson et al. and Elliot. This would have been obvious in order to provide a method of ensuring that a communication link (or bus) is operating properly, and prevent the system from wasting time sending messages to processors/terminals that are not responsive (column 14, lines 11 – 19).

* * *

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (U.S. 6,122,758) in view of Elliot (U.S. Pub. 2005/0055489) and Yoshida (U.S. 5,928,372).

Johnson et al. and Elliot fail to teach wherein the receive machine comprises checksum generation means for generating a message checksum for a message while the message is being received by the bus controller over the system bus.

Yoshida teaches a checksum generation means for generating a message checksum for a message while the message is being received by the bus controller over the system bus (where checksum generation means may be interpreted as data check code generation circuits; column 11, lines 14 – 24).

It would have been obvious to one or ordinary skill in this art at the time of invention by applicant to combine the checksum generation means of Yoshida with the system of Johnson et al. in order to provide for a means of verifying the data transmitted across the system bus. This would have been obvious since error-free data is critical to the correct operation of a digital system.

* * *

Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Elliot and Cao et al.

Regarding claim 44, Johnson et al. teach a device for use in a computer system including a system bus (Figure 4, 7, item 310; column 7, lines 10 - 12) and a bus controller coupled to the system bus (where a bus controller may be interpreted as a system interface processor; column 11, lines 31 – 36, 61 - 65).

A send machine (Fig. 7, item 707) and a FIFO buffer coupled to the send machine (Fig. 7, 516), however Johnson et al. fails to teach the send machine and FIFO buffer connected as recited in the claim, as well as the first and second internal buses.

Elliot teaches a bridge circuit which could be implemented in a system such as that of Johnson et al. for the purpose of allowing components to operate at different clock rates (par. 4). This circuit could be implemented in Johnson et al., for example, in the location of items 514 and 516 in Figure 7 to allow the system interface processor (312) and host processor (200) to operate at different clock rates. Thus, the

combination of Johnson et al. and Elliot teaches a send machine (Elliot: 68) coupled between a host processor (Johnson: 200) and the bus controller (Johnson: 312) over a second internal bus (Elliot: l-data, t-data, l-add, t-add); and a first first-in first-out (FIFO) buffer (Elliot: 60) coupled to the send machine (Elliot: 68), the first FIFO further coupled in parallel with the send machine (as shown in Elliot, Fig. 2) between the host processor (Johnson: 200) and the bus controller (Johnson: 312) over the first internal bus (Johnson: 226) but not over the system bus (Johnson: 310).

Additionally, Elliot teaches A receive machine (70)) coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor (par. 6, par. 34); and a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller (62) over the **third** internal bus (l-r-data, t-r-data), the second FIFO not being coupled to the receive machine over the second internal bus (as shown in Fig. 2) but not over the system bus (as shown in Fig. 2), the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor (par. 44).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the bridge circuit as taught by Elliot into the system of Johnson et al. for the purpose of allowing different components on the bus to correctly operate at different clock rates (par. 4). This would have been obvious since Elliot teaches that it is advantageous to operate components at different clock rates in an integrated circuit (par. 4).

Johnson et al. and Elliot fail to describe a busfree count means, a busfree timer, and a fair arbitration block.

Cao et al. teach:

A busfree count means for storing a busfree count (where a busfree count may be interpreted as an arbitration count number; column 4, lines 42 – 50);

A busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use (where a busfree timer may be interpreted as a “quiet slot” counter; column 4, lines 51 – 60);

A fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal (where a busfree count may be interpreted as an arbitration count number; column 5, lines 59 – 64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the busfree count and busfree timer as taught by Cao et al. into the system of Johnson et al. and Elliot for the purpose of providing arbitration amongst devices on the system bus. This would have been obvious since Cao et al. teach that their invention provides for more efficient use of bus bandwidth (column 10, lines 25 – 59), along with permitting data communication with a very small probability of data collisions (column 4, lines 32 – 34).

Response to Arguments

Applicant's arguments filed 6/21/2007, with respect to the rejection(s) of claim(s) 1 – 13 and 42 – 44 under Johnson et al. have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Johnson et al. (U.S. 6,122,758) in view of Elliot (U.S. Pub. 2005/0055489).

Elliot teaches a FIFO coupled in parallel with a send machine (Fig. 2, items 60, 68).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier system from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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